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Analysis,Modelling and Simulation of a Multiphase Interleaved Buck Dc/Dc Converter for PV Applications

Khaled N. Faris ,HalaS. Khalil, and Mohsen M. T. EL-Hagry
Power Electronics and Energy Conversion Dept., Electronics Research Institute, Tahrir Street, Dokki, Giza, Egypt.
Emails: khalederi@yahoo.com,hala_shaban@eri.sci.eg, elhagry_251@yahoo.com

Abstract:The Continuous Advances in Power electronics technologies and regulation systems have provided an opportunity for designing of efficient Converters for charging process of storage elements, especially in photovoltaic (PV) systems, these converters must have a minimum ripples contents, this can be achieved by using advanced multiphase interleaved DC/DC converters. These converters are used to regulate the output voltage and current of the PV – charging system to obtain an efficient charging /discharging process for direct Energy Storage Systems (ESS), also control the power flow and track the maximum power of the PV modules. In this paper, a design and implementation of a multi-phase interleaved Buck DC/DC converter is introduced for obtaining an efficient PV Battery charging system. Also a comparison between the conventional single phase and the proposed multi-phase interleaved topology is recorded.

Keywords: **Buck Converter, Interleave Topology, ripples reduction, PV Systems.**

I. INTRODUCTION

– Problem definition and work motivation:

In PV systems, the direct energy storage systems (ESSs), such as Lead Acid Batteries (most mature technology) play a vital role in such systems. To Keep and extend the life time of such storage elements, charging process is considered one of the most important factors that affect the life time of those batteries.The charging process includes two issues, the 1st issue subjects to the different charging modes of Lead Acid Batteries for PV applications as in [1], and the 2nd issue concentrates on the charging current quality for ripples contents, which plays a vital role for life time and aging for such batteries.

Hence, this research aims to reduce the current ripples of the charging converters. These converters usually used with PV systems may be buck, boost, or buck-boost converters that are characterized by plenty of ripples content that affect seriously the life time of chemically storage devices, such as lead acid batteries.

Here, in this work an interleaved topology of buck DC/DC converter for PV charging system is proposedto achieve an efficient charging process, while minimizing the ripple contents in the charging current.

II. PV SYSTEM

The PV cell is modelled by a current source in parallel with a diode [1] is shown in Figure (1).

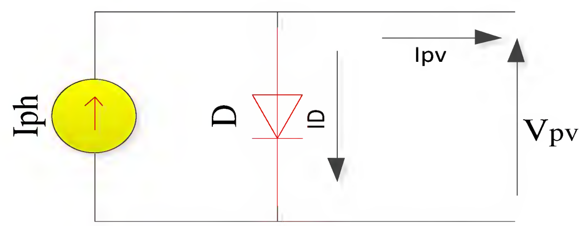


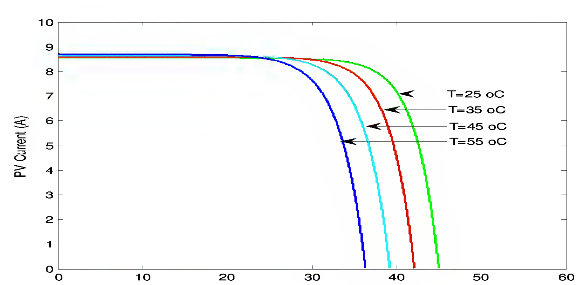
Figure 1: Equivalent circuit of a PV cell.

The electrical characteristics of the PV cell are nonlinear and vary according to the solar insolation (G) and the cell temperature (T). The output current from the PV cell Ipv can be expressed by equation 1

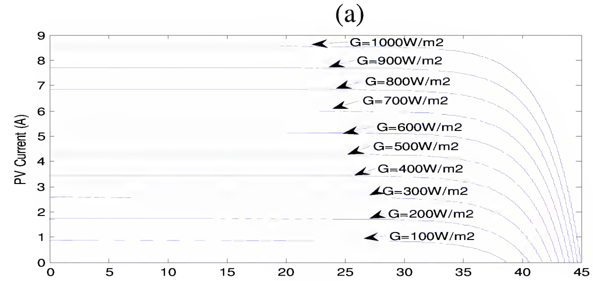
$$I_{pv} = I_{ph} - I_0[exp\ (\frac{Q.V_{pv}}{A.k.T}) - 1] \qquad (1)$$

WhereIphisthe photo generated current, Io is the dark saturation current, Q is the electron charge =1.6*10-19 (C), Vpv is the output voltage of the PV cell, A is the ideality factor of the diode, K is Boltzmann constant =1.38*10-23 (J/K), T is the cell temperature (oC). The output current of a PV module integrates a number of cells connected in series (Ns) and number of cells connected in parallel (Np) can be expressed by equation 2. The simulated electrical characteristics of the adopted PV module are shown in Fig. 4.

$$I_{pv} = N_p.I_{ph} - N_p.I_0[exp\ (\frac{Q.V_{pv}}{N_s.A.k.T}) - 1] \qquad (2)$$



(a)



(b)

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Figure 2: (I-V) curve ofIS4000PV module (a) at different Temperatures (b) at different solar insolation [2]

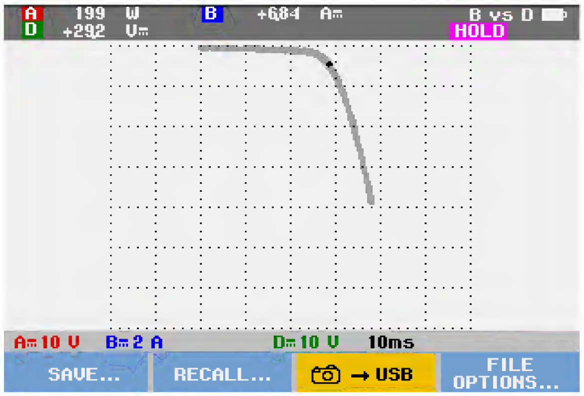

Figure 3: Lab. Characterization of the adopted PV module.

- **Maximum Power Point tracking technique**

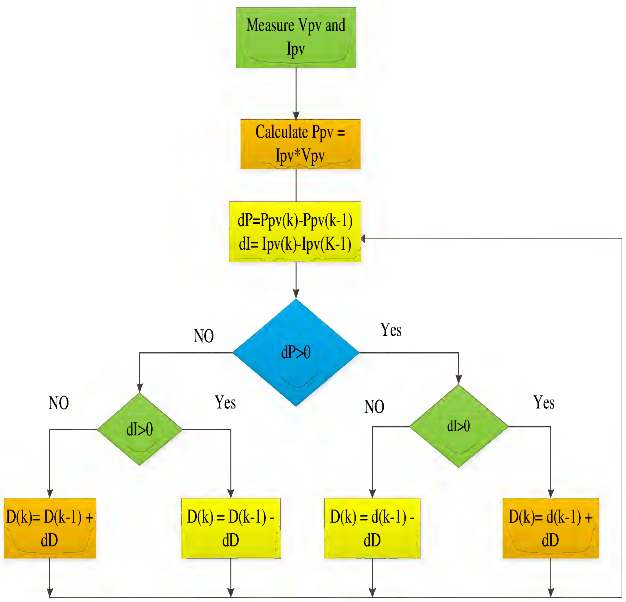

Figure 4: Flow chart for the Modified Perturb and observe (P&O) algorithm for MPPT [2].

The modified Perturb and observe Maximum power point tracking technique is carried out as in [2], the flow chart of the MPP tracking technique is shown in figure 3. The MPP tracker enables the converter to be able to draw a maximum power from PV module by adjusting the duty cycle of the converter.

$$dP = P_{pv}(k) - P_{pv}(k-1) \quad (3)$$

$$dI = I_{pv}(k) - I_{pv}(k-1) \quad (4)$$

The output variable is*dD,* which is given by:

$$dD = D(k) - D(k-1) \quad (5)$$

Where *dP* is change in PV power, *dI* is the change in PV current and *dD* change in duty cycle, *D(k)* is the current duty cycle, *D(k-1)* is the previous value of the commanded duty cycle.

The maximum power point tracker searches for the MPP through the adopted modified P&O algorithm shown in figure (3).

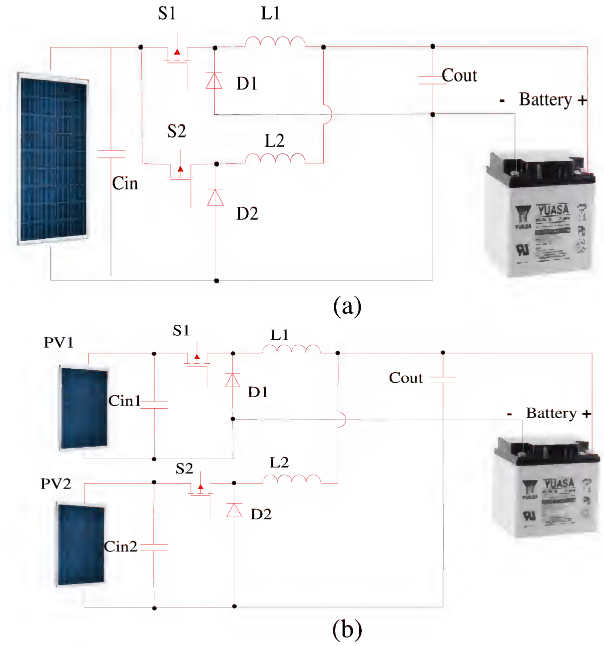

Figure 5: two phase-interleaved buck converter with (a):one source (b): two sources.

The samemodified P& O algorithm is applied for the proposed Multiphase interleaved buck DC/DC Converter (MIBC) by shifting the generated PWM signals by $360^{o}/n$, where n: is number of phases of the (MIBC). So, if a two phase MIBC, The inductor phase currents are interleaved by delaying the gating signals to the switching elements by $360^{o}/2$, which equals 180^{o}, for three phases MIBC, the delay is 120^{o}.

II –MULTI-PHASE INTERLEAVED BUCK DC/DC CONVERTER

Single phase buck converters are considered a source of ripples; this ripple content is not recommended for charging the storage elements in PV system applications. The presence of the ripple content reduces the charging / discharging efficiency of direct energy storage systems (ESS).

Also, in high current applications, the efficiency and power dissipation becomes a vital issue. One of the effective solutions for the above mentioned issues is the using of multi-phase buck DC/DC converter for ripples reduction, also for increasing the efficiency of the charging /discharging process of the storage elements in PV systems.

In addition, Multi-phase interleaved Buck Converters (MPIBCs) reduces the RMS current power dissipation in power switches and inductors [3].

The input inductance aid in controlling the current ripple and has a positive effect on reducing the reducing electromagnetic emissions. However the inductor size is proportional to the inductance and peak current square. For high power applications, the size of the inductor is considerable.

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Hence, the development of new technique is considered essential to reduce the ripples and limit the associated electrical stresses.

Recently, an efficient multi-phase interleaved DC/DC converter topology has many benefits compared to the conventional topologies, such as, reduction of passive component's size (Inductors and capacitors), reduction of input and output waveforms ripples, increasing of converter power rating, and reduction of the rating of the active power switches. The interleaving power converters are achieved through paralleling of multiple switching converters. The switching frequencies are identical, but the switching instants are sequentially phased over equal fractions of the switching period [4].

In [5] a multi-phase interleaved buck converter is introduced for supplying the microprocessors with an efficient and minimum ripples power supplies.

Many literatures handled the effect of the ripple currents on the performance and aging of the energy storage systems (ESS), such as [6].

III – ELEMENTS DESIGN OF THE PROPOSED INTERLEAVED BUCK CONVERTER

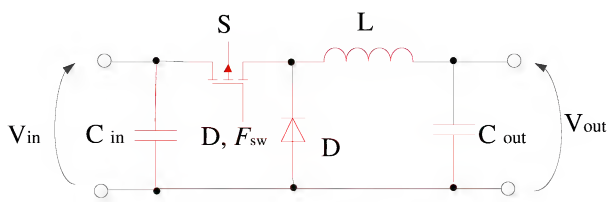

Figure 6: Single Phase Buck Converter – Basic Diagram.

A single phase buck converter is the most basic switched mode power supply (SMPS) topology. It is widely used throughout the industry to convert a higher input voltage into a lower output voltage. The buck converter (voltage step-down converter) is a non-isolated converter, hence galvanic isolation between input and output is not given [7].

The single phase buck converter consists of one controlled active switch (S1), a rectifier (D1) and filter elements (L1 and C2). This great simplicity allows for cost effective high efficient power distribution throughout the application. It has the filter inductor (L1) on the output side, which provides a smooth continuous output current waveform to the load.

PV module Maximum Power	300 W
Input voltage at MPP of PV module	37.6 V
Current at MPP of PV module	7.976 A
Output Voltage	24 V
Switching Frequency	10 KHZ
Inductor current ripple	30 %
Output voltage ripple	10 mV
Max.UsedNo. of Phases	3

3-1 Filter inductor design:

In the adopted charging system from IS400P PV module with 37.6V, and 7.796A at maximum power point to charge two 12V, 50 Ah Lead Acid Batteries, with a maximum output current around 12.5 A, which equivalent to C/4, where C is the rated capacity of the used Lead Acid batteries.

The switching frequency is selected at 10 kHz and the current ripple will be limited at 30 % of maximum load current. The value of the filter inductor is calculated from equation (6) as mentioned in [8]:

$$L = \frac{(Vin - Vout) * D}{\Delta I * fsw} \quad (6)$$

Where: L: inductance of the filter inductor, V_{in}: input voltage, $\Delta I = 0.3 * (I_{Max\_out})$, V_{out}: Output voltage, D: maximum duty cycle, and η : Converter efficiency.

$$MaxDutyCycle\ (D) = \frac{V_{out}}{V_{in\,(Max)} * \eta}$$

Where:
Vin(Max): Maximum input Voltage.
Vout: Output Voltage.
η: Efficiency of the converter.

$$\Delta I_L = \frac{V_{in\,(max)} - V_{out}}{f_s * L} * D \quad (7)$$

$$L = \frac{\left(V_{in\,(max)} - V_{out}\right) * D}{f_s * \Delta I_L} \quad (8)$$

The higher the inductor value, the higher is the max Output current because of the reduced ripple current as

$$I_{max\,(out)} = I_{LIM(min)} - \frac{\Delta I_L}{2} \quad (9)$$

ΔI_L=estimated inductor ripple current.

The inductor ripple current cannot be calculated with equation (6) because the inductor is not known. A good estimation for inductor current is 20% to 40% of the output current [5].

Where: ΔI_L=estimated inductor ripple current.

$I_{out(max)}$= maximum output current necessary in the application (charging).

Output capacitor: for interleave, the function of the output capacitor is to filter the inductor current ripple and deliver stable output voltage.One criterion defines the value and concrete design of the output capacitor solution is [5].

$$C_{out(min)} = \frac{1 - D}{\frac{\Delta V_{Cout}}{V_{out}} * 8L * (n.f_{sw})^2} \quad (10)$$

Where ΔV_{Cout}=change in the output voltage ripples.
n= No. of phases.

Input capacitor

The function of the input capacitor is to filter the input current into the regulator-ideally. It should appear as a DC current for steady state load conditions.

$$I_{in} = \frac{D}{\eta}.I_{out} \quad (11)$$

$$C_{in} \geq \frac{I_{out}\left(\frac{D}{n} - D^2\right)}{\eta . f_{sw} . dV_{in}} \quad (12)$$

Where:
dV_{in}:is the permissible voltage ripple at the input capacitor.

$$P_{C_{in_{loss}}} = I^2_{C_{in}}.ESR \quad (13)$$

$$I_{C_{in}} = \frac{I_{out}}{\eta}.\sqrt{\frac{D}{n^2} - \frac{D^2}{n}} \quad (14)$$

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SWITCHING MOSFET SELECTION:

1- The buck converter is a hand switched topology. The switching MOSFET has to resemble an ideal switch, i.e. being low Ohmic and fast switching. Also Selection a P-Type is preferable for ease of driving gate, with low R_{ds}

$$ESR_{Cout} = \frac{1}{\Delta I_{inductor}} * \left(V_{out_{ripple}} - \frac{1}{2C_{out}} * \frac{V_{in_{max}} - V_{out}}{L}\left(\frac{V_{out}}{V_{in_{max}}} * \frac{1}{f_{sw}}\right)^2\right) \quad (15)$$

[9]

$$C_{in} = (10\mu F - 22\mu F)/Ampere\,Of\,I_{output}. \quad (16)$$

$$(10\mu F - 22\mu F) * I_{output} \quad (17)$$

- Diode Selection:

$$P_{Diode} = \left(1 - \frac{V_{out}}{V_{in}}\right) * I_{out\,(max)} * V_D \quad (18)$$

- For reliable operation over the input voltage range, the reverse – repetitive maximum voltage is greater than the Maximum input voltage $V_{RRMV} \geq V_{inMax}$.
- The Diode's forward current must meet or exceed the maximum output current. $I_{FAV} \geq I_{out\,(MAX)}$

IV- SIMULATION RESULTS:

A simulated modelling for the interleaved topology shown in figure (5a) for a buck converter is carried out using MATLAB /Simulink. The results are recorded for a conventional Buck converter, 2-phase interleaved topology, and a 3-phase interleaved buck converter. The results are shown from figure (7-9), the current ripple is recorded in (a), also the carrier, and gating signals are recorded in (b), and (c).
From the analysis of results, it is clear that, there is a noticeable reduction in current ripples, especially in 3-phase configuration as in figure (9). Also, the passive elements sizes are reduced, as in conventional configuration, the used output capacitor is 3500 micro-farads, but in 3-phase configuration is 350 micro-farads as calculated from equation (5). The used inductance is 0.3milli-henery (mH) as calculated from equation (1. Also the input capacitor value is reduced by increasing the number of phases as in Equation (7).Figure 10 shows the currents in individual phase against the total output current from the three phase interleaved buck converter used for PV battery charging. Figure 11a, and b shows the simulated PV battery terminal voltage and the state of chargeof Two12V, 50Ah batteries model (YC50-12) during charging process using the proposed topology for the charging converter.

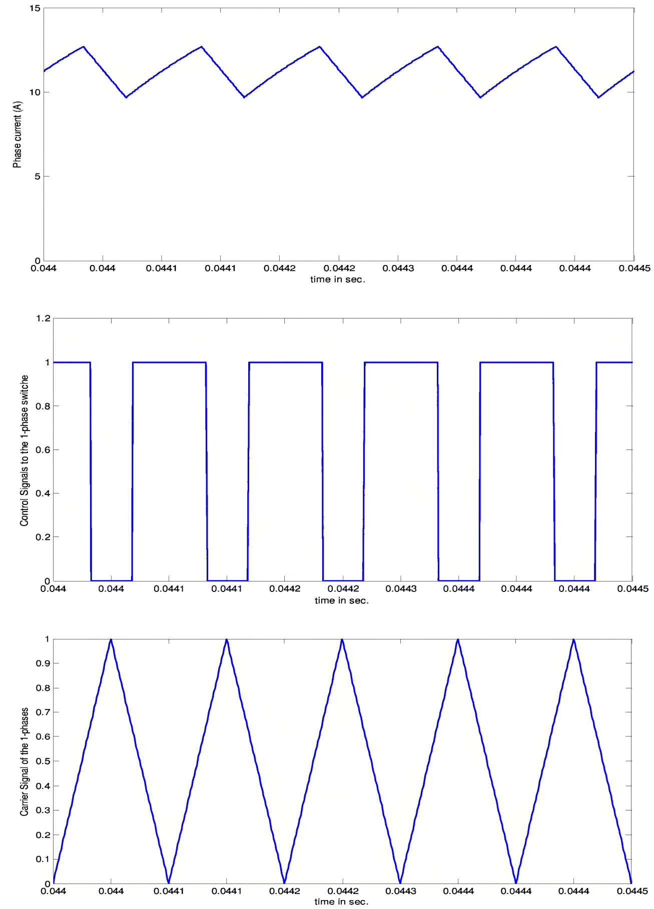
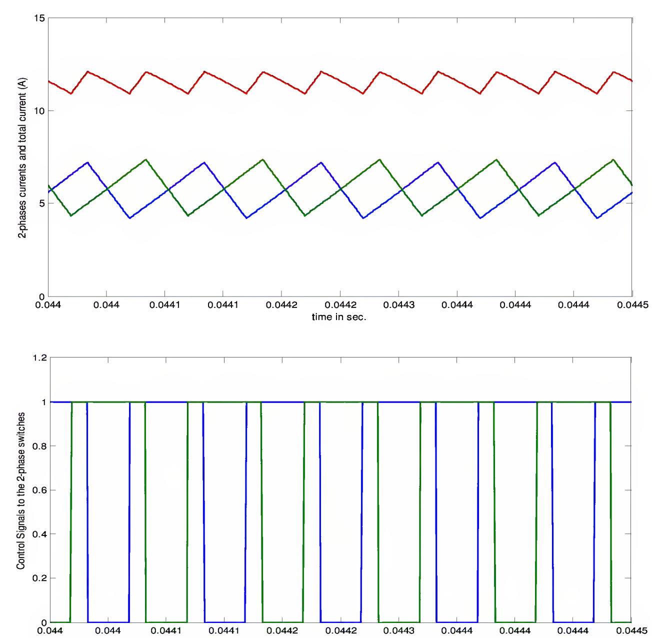


Figure 7: (a) Output current from conventional Buck converter, (b) driving signal, and (c) carrier signal



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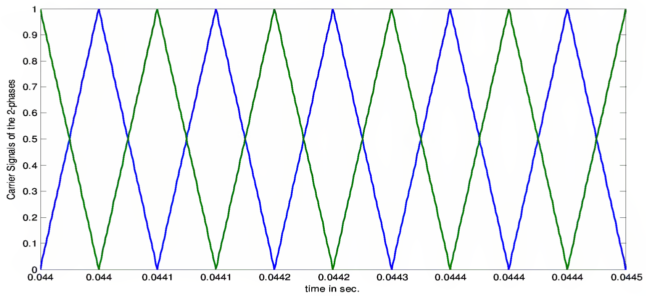
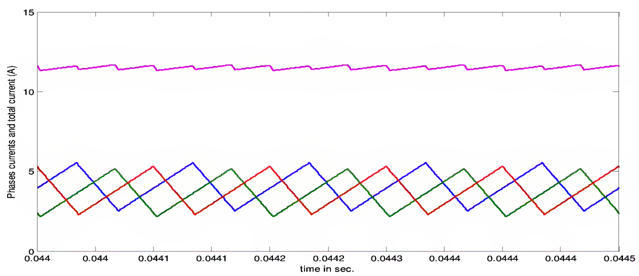
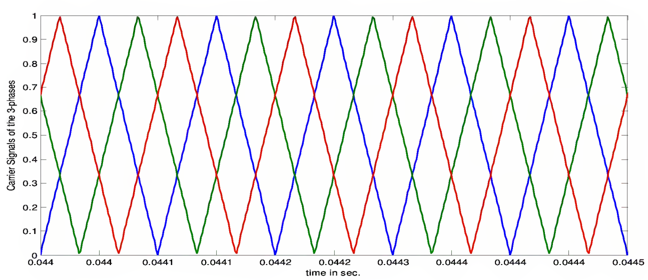


Figure 8: (a)output current from 2-ph interleaved Buck converter, (b) gating signals (180^o shift), and (c) carrier signals (180^o shift)



(a)



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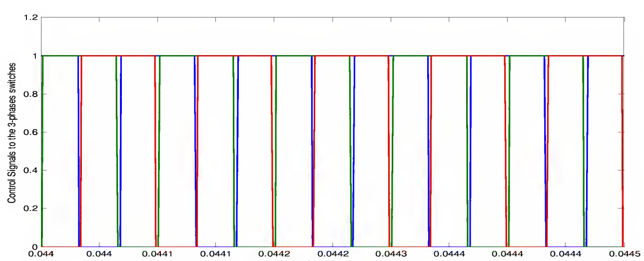


(c)

Figure 9: (a)Output current from 3-ph interleaved Buck converter, (b) carrier signals (120^o shift), and (c) gating signals (120^o shift)

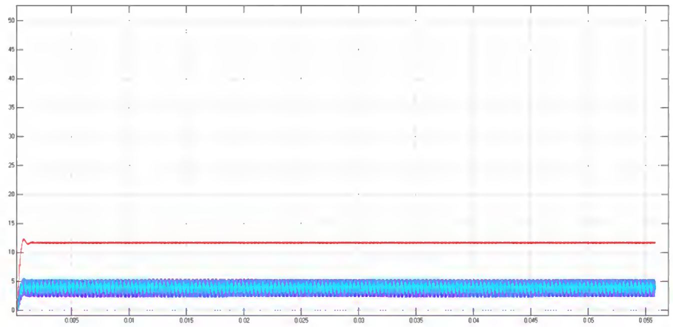
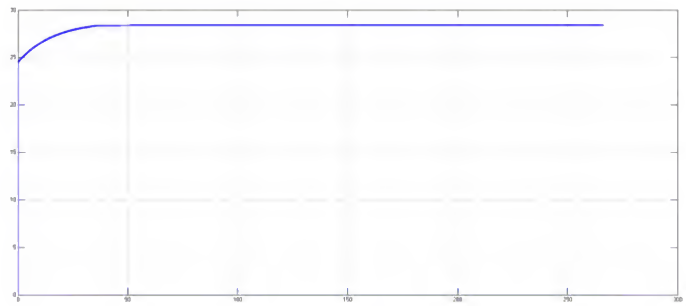
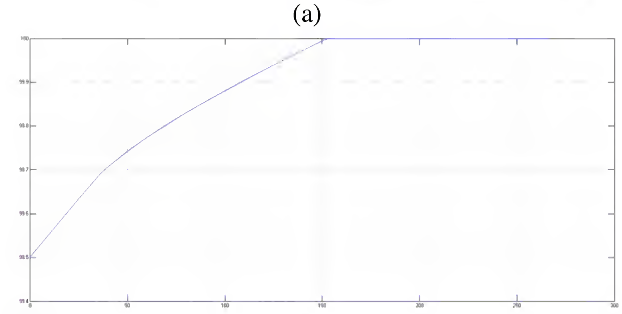


Figure 10: The three Phases currents against the total output current.



(a)



(b)

Figure 11: (a) Simulated battery terminal voltage and (b): The State of charge (SOC) during charging process for two batteries of12V each.

VI- EXPERIMENTAL RESULTS

A Lab Scale Experimental results are recorded for a conventional buck converter with the designed parameters as shown in figure 12.Also the proposed topology is verified experimentally as shown in figure 13, and 14. The experimental results show a good agreement with the Idea of the proposed configuration.

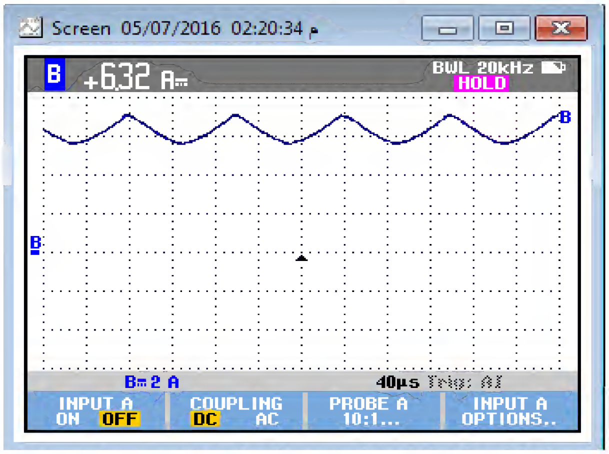


Figure 14: output current for the Conventional Buck with the designed parameters.

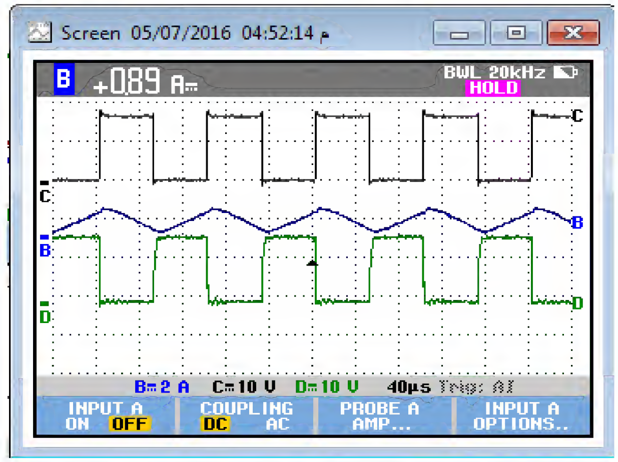
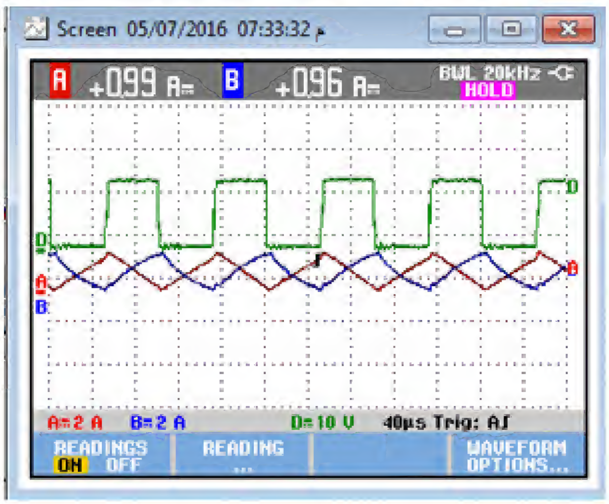
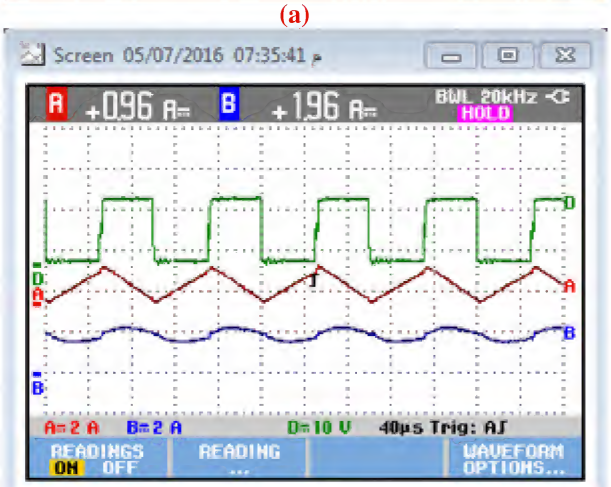


Figure 14: Driving signals for the two switches (Channel C, and D)



(a)



(b)

Figure 13: (a): Two phases current (Channel A and B)(b): Total current on(Channel B)

V- CONCLUSIONS

Design, modelling and simulation of an interleaved buck DC/DC converter for PV battery charging system has been proposed. Also an output current with a minimum ripple content has been recorded by using the proposed topology. The second issue for charging of PV batteries has been discussed. By using the introduced topology, the passive elements sizes have been reduced. The proposed configuration provides a high reliability for PV systems, especially for the chemically storage devices such as Lead acid batteries, which are considered the most matured storage elements for PV systems.A Lab scale Experimental results for two phases configuration have been obtained for design verification of the proposed interleaved topology.

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